Amendments to the Claims:

1. (canceled)

2. (canceled)

3. (canceled)

4. (canceled)

5. (currently amended) A MOS transistor with reduced drain capacitance comprising

a drain, and

a lateral isolation trench extending at least partially underneath the drain ~~A MOS of claim 4~~, wherein the trench is filled with ~~insulator is~~ PETEOS.

6. (currently amended) A MOS transistor with reduced drain capacitance comprising

a drain, and

a lateral isolation trench extending at least partially underneath the drain ~~A MOS of claim 1~~, wherein the trench has a <110> orientation.

7. (original) A MOS of claim 6, wherein the trench is formed in a <100> silicon wafer.

8. (canceled)

9. (canceled)

10. (currently amended) A method of forming a laterally extending trench in a semiconductor material underneath a drain of a MOS transistor, comprising

choosing a predetermined crystal orientation,

etching a vertically extending STI region next to the drain, and

using an anisotropic etchant to etch a trench extending laterally from the STI, wherein ~~A method of claim 8, wherein the~~ choosing of the crystal orientation includes choosing a lateral trench direction that is in the <110> direction.

11. (original) A method of claim 10, wherein the semiconductor material is silicon.

12. (original) A method of claim 11, wherein the etchant is a wet anisotropic silicon etchant.

13. (original) A method of claim 12, wherein the etchant includes KOH.

14. (original) A method of claim 13, wherein the etchant further includes alcohol and water.

15. (original) A method of claim 12, wherein the etchant includes TMAH.